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10/801,260

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Ichiro Fujimori

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11/28/2006

MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER

CAO, PHAT X

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/801,260

Applicant(s)

FUJIMORI, ICHIRO

Examiner

Phat X. Cao

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 8-9, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puar et al (US. 6,356,497) in view of McCormack et al (US. 6,395,591).

Regarding claims 1 and 8-9, Puar (Fig. 5) discloses a system for reducing noise in a chip, the system comprising: a substrate layer (P substrate) integrated within the chip; a transistor well layer (N-Well) integrated within the chip; at least one transistor of a first transistor type (P-type) formed within the well layer; and a positive potential of a quiet voltage source Vdd (column 4, lines 59-63) that is coupled to the at least one transistor of the first transistor type.

Puar does not disclose that the transistor well layer (N-Well) is shielded by a shielding layer.

However, McCormack (Fig. 2) teaches the forming of a transistor within a transistor well layer and on a lightly doped (p-) substrate layer 50. The transistor well layer is isolated or shielded from the substrate 50 by a p type epitaxy layer 12 disposed therebetween. The layer 12 functions as a shielding layer for reducing the noise in the chip because it isolates the substrate 10 from the transistor layer and has a higher

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doping than the underlying substrate 10 for providing immunity against parasitic substrate effects or latchup effects (column 1, lines 19-24 and column 4, lines 9-13). Accordingly, it would have been obvious to modify the device of Puar by forming the shielding layer between the substrate layer and the transistor well layer because such forming of the low resistivity shielding layer would isolate the noise transfer to the transistor layer by reducing parasitic substrate effects or latchup effects.

Regarding claims 14-15, Puar (Fig. 5) further discloses a noisy voltage source 38 of positive (column 4, lines 59-63) coupled to a source of the transistor.

Regarding claim 12, McCormack (Fig. 2) further teaches that the shielding layer 12 is disposed between the substrate layer 10 and the transistor well layer 16/18/22.

3. Claims 1-10, 12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al (US. 6,395,591) in view of Puar et al (US. 6,356,497).

Regarding claims 1, 8-9 and 12, McCormack (Fig. 2) discloses a system for reducing noise in a chip (column 2, lines 45-50), the system comprising: a substrate layer 10 integrated within the chip; a transistor well layer 16/18/22 within the chip, which is isolated or shielded from the substrate layer 10 by a shielding layer 12; a transistor 30 of a first transistor type (P type) disposed within the transistor well layer 22, wherein the transistor well layer 22 is coupled to the shielding layer 12, and the shielding layer 12 is disposed between the substrate layer 10 and the transistor well layer 22.

McCormack does not disclose a positive potential of a quiet voltage source coupled to the transistor 30.

However, Puar (Fig. 5) teaches the forming of a system for reducing noise in a chip, the system comprising a transistor of P type disposed in a transistor well layer (N-Well) and having a positive potential V_{dd} of a quiet voltage source (column 4, lines 59-63) coupled to the transistor. Accordingly, it would have been obvious to couple a positive potential of a quiet voltage source to the transistor well layer (N-Well) of the transistor 30 of McCormack because such coupling of positive quiet voltage source to the transistor well layer would prevent the noise generated from the noisy substrate voltage, as taught by Puar (column 4, lines 55-65).

Regarding claims 2-7, McCormack (Fig. 2) further discloses a transistor 28 of a second transistor type (N type) disposed within the transistor well layer 16 and coupled to the shielding layer 12, wherein the transistor 28 has a transistor well layer 16 of P type is resistivity coupled to the shielding layer 12 of P type and has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28.

Regarding claim 10, McCormack (Fig. 2) further discloses that the transistor 30 has a transistor well layer 22 of N type is capacitively coupled to the shielding layer 12 of P type.

Regarding claims 14-15, Puar (Fig. 5) also teaches a noisy voltage 38 (column 4, lines 59-63) coupled to the transistor source of a first transistor type (P type).

4. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al and Puar et al as applied to claim 1 above, and further in view of Wei (US. 6,403,992).

McCormack discloses the shielding layer 12 is deep P-well, but not N-well which

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is capacitively coupled to the substrate layer 10.

However, Wei teaches the conventional of forming a transistor within a shielding layer of P-well, which is capacitively coupled to the N type substrate (Fig. 3), or a transistor within a shielding layer of N-well, which is capacitively coupled to the P type substrate (Fig. 4). Accordingly, it would have been obvious to form the shielding layer 12 of McCormack with either N type or P type because they both provide the benefits of eliminating substrate effect, as taught by Wei (column 1; lines 47-60).

5. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei (US. 6,403,992) in view of Puar et al (US. 6,356,497).

Regarding claims 1, 8 and 13, Wei (Fig. 4) discloses a system for reducing noise in a chip, the system comprising: a substrate layer integrated within the chip; a transistor layer 46 integrated within the chip, which is shielded from the substrate layer by a shielding layer N-well 484, wherein the shielding layer N-well 484 reduces the transfer of noise or body effect in the chip (column 1, lines 55-60); a transistor G4 of a first transistor type (p type) that couples the transistor layer 46 to the shielding layer 484; and a positive potential Vcc (+5V) of a voltage source coupled to the transistor G4.

Wei does not disclose that the positive potential Vcc (+5V) is a quiet voltage source.

However, Puar (Fig. 5) teaches a system for reducing noise in a chip, the system comprising a quiet positive potential Vdd (column 4, lines 59-65) coupled to a transistor layer N-well of the P-type transistor. Accordingly, it would have been obvious to connect the positive potential Vcc of the P-type transistor G4 of Wei to a quiet voltage

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source in order to provide a "quiet" transistor layer which isolates the transistor from the "noisy" substrate voltage, as taught by Puar (column 4, lines 59-65).

Regarding claims 2-7, Wei (Fig. 4) further discloses: a second transistor G3 of N-type disposed within the transistor layer 46 and resistivity coupled to the N-well shielding layer 484; and a first noisy voltage source GND (0V) coupled to a source S3 of the second transistor type G3.

Regarding claims 9-10 and 11-12, Wei (Fig. 4) also discloses: the first transistor G4 of P-type disposed within the transistor layer 46 and capacitively coupled to the N-well shielding layer 484; and the N-well shielding layer 484 capacitively coupled to the P-type substrate layer and disposed between the substrate layer and the transistor layer 46.

Response to Arguments

6. Regarding the rejections on claims 1-10, 12 and 14-15, Applicant asserts that "since epitaxial substrates have a low bulk resistivity material underneath the epitaxial layer, the epitaxial layers will couple noise more efficiently to nearby circuits or layers". Applicant then concludes that the epitaxial layer 12 of McCormack does not function as a shielding layer.

This argument is not persuasive because of the following reasons:

First, it is noted that the statement asserted by Applicant above is clearly applied when the substrate underneath the epitaxial layer has a resistivity lower than the resistivity of the epitaxial layer. However, it is not applied to the substrate and the epitaxial layer of McCormack because the substrate 10 does not have a resistivity lower

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than the resistivity of the epitaxial layer 12, but rather, the substrate 10 has a resistivity higher than the resistivity of the epitaxial layer 12 because the substrate (P-) has lower doping than the epitaxial layer 12 (P);

Second, McCormack states that "the high substrate resistance renders the integrated circuit more susceptible to latchup" (column 1, lines 22-24), and further states that "A conventional way to reduce latchup susceptibility is to lower the resistance of the P-wells" (column 4, lines 8-10). Accordingly, the forming of the layer 12 between the well layers and the substrate 10 would reduce the parasitic resistance effects and the parasitic capacitance effects formed between the well layers and the substrate 10 because the layer 12 (P- doping) shields the well layers from the substrate 10 and has a resistivity lower than the resistivity of the substrate 10 (P doping). Therefore, the layer 12 is a shielding layer for reducing the noise in the chip because it has properties of enhancing latchup suppression formed between the well layers and the high resistivity substrate 10; and

Third, it should be noted that the arguments of counsel cannot take the place of evidence in the record. In re Schulze, 346 F.2d 600, 602, 145 USPQ 716, 718 (CCPA 1965). Attorney statements are not evidence and must be supported by an appropriate affidavit or declaration. See M.P.E.P. 716.01(c). In this case, Applicant has failed to provide the evidence to support that the layer 12 is not a shielding layer for reducing latchup or noise even though it shields the well layers from the high resistivity substrate and it has a resistivity lower than the resistivity of the substrate.

Regarding the rejections on claims 11 and 13, Applicant argues that the N-well layer 484 of Wei acts as a shielding layer to reduce the "body effect", but not reduce "noise" in the device.

This argument is not persuasive. Based on Webster's II New College Dictionary, "noise" is defined as "A usu. Random and persistent disturbance that obscures or reduces the clarity or quality of a signal" (see attached papers). Therefore, the "body effect" is a "noise" effect because the "body effect" would also reduce the clarity or quality of a signal.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703.

The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
November 21, 2006



PHAT X. CAO
PRIMARY EXAMINER